impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode.

21. (Amended) A semiconductor device comprising:

an element substrate including a semiconductor layer of a first conductivity type being formed over a semiconductor substrate with a dielectric film interposed therebetween;

said element substrate having a groove formed therein with a depth extending from a top surface of said semiconductor layer into the inside of said semiconductor substrate after penetration through said dielectric film, said groove being formed to have an increased width portion in said dielectric film, said dielectric film of said increased width portion being receded laterally as to expose a bottom surface of said semiconductor layer and such that the width of said groove in said dielectric film is greater than that of said groove in said semiconductor layer;

a trench capacitor formed under said dielectric film to have a storage electrode as half buried in said groove;

an impurity diffusion source buried in said increased width portion of said groove to serve as a buried strap, bottom surface and top surface of said impurity diffusion source being contacted with said storage electrode and said bottom surface of said semiconductor layer, respectively;

a cap insulation film formed in said groove to cover said impurity diffusion source; and

a transistor having a first diffusion layer of a second conductivity type being formed through impurity diffusion from said impurity diffusion source to said bottom surface of said semiconductor layer, a second diffusion layer of the second conductivity type formed through impurity diffusion to said top surface of said semiconductor layer, and a gate electrode formed at a side face of said groove over said impurity diffusion source with a gate insulation film between said side face and said gate electrode, said transistor constituting a DRAM cell with said trench capacitor.

Please see the attached Appendix for the changes made to effect the above claims.